Tom Edgar's Contributions to the Semiconductor Industry: From Controlling Processes to Technology Development

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Background

- Born in Bartlesville, OK
- Undergraduate ChE at the University of Kansas
- Attended “elite” graduate school
- Settled in Texas

Outline

- Automated Process Control at Texas Instruments Inc
- Broad application of generic APC algorithm
- Economic Impact
- Historical Perspective
- Recent Advances

Definition of Process

- http://dictionary.reference.com/
  - 1. a systematic series of actions directed to some end
- In ChE terms, A “process” is a batch chemical reaction
- Integrated circuits are manufactured on top of silicon wafers with a series of deposition, pattern, and etch processes
  - 1200 - 2200 processes to manufacture an IC
  - 180 – 300 unique processes
- These batch chemical reactions require expensive, sophisticated equipment and are much more complex than one would gather by examining run-to-run control algorithms
- Control does not necessarily imply feedback

Process Engineering

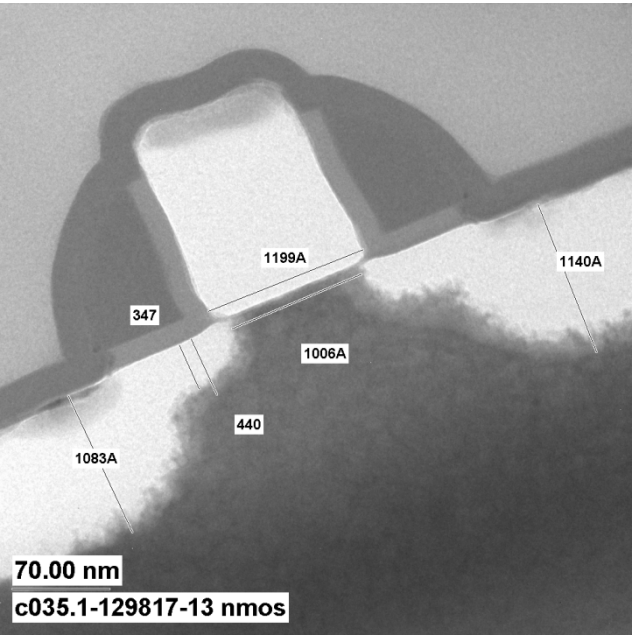
- A group of Process Engineers (PE) maintain the recipes to support the manufacturing processes in each fab
  - Photolithography
    - Reticles, photoresists and tracks, align & exposure tools
  - Etch
    - Plasma etches for dielectrics, silicon, metal; photoresist ashing
  - Thin Films
    - Plasma Enhanced, sputter, and electroplated depositions
  - Diffusion
    - Multi-wafer Furnaces, Single wafer Lamp Heated chambers
    - Ion implantation and anneal
  - Chemical Mechanical Polishing
    - Oxide, copper, tungsten
  - Surface preparation
    - Passivation, cleaning

Example: Gate Etch Process

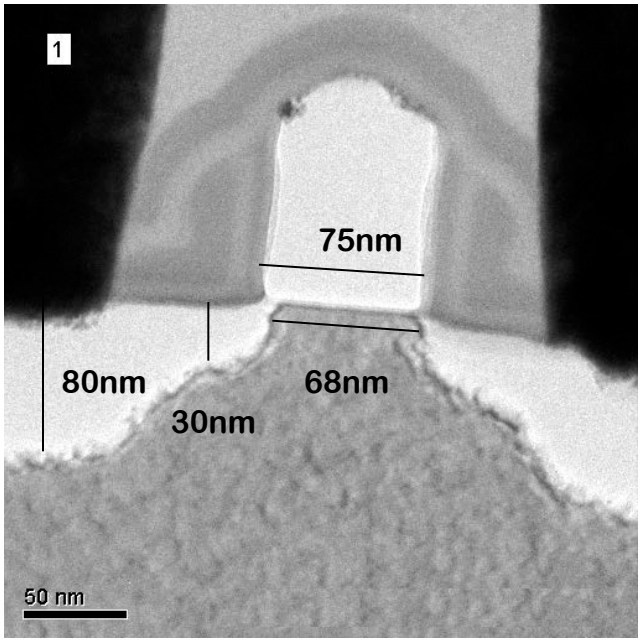
- The most critical process for defining the transistor gate length, which is primarily responsible for transistor performance
- 65 nm node recipe has 34 header variables, 18 steps with 53 variables per step
- Source power, bias power, rf frequency, gas chemistry, flowrates, etc. are optimized by process development engineer to provide a good poly profile
  - A 65 nm printed linewidth can be etched down to a poly linewidth ~40 nm
- One of 988 recipes variables (resist trim time) is manipulated with APC

Gate Cross Sections

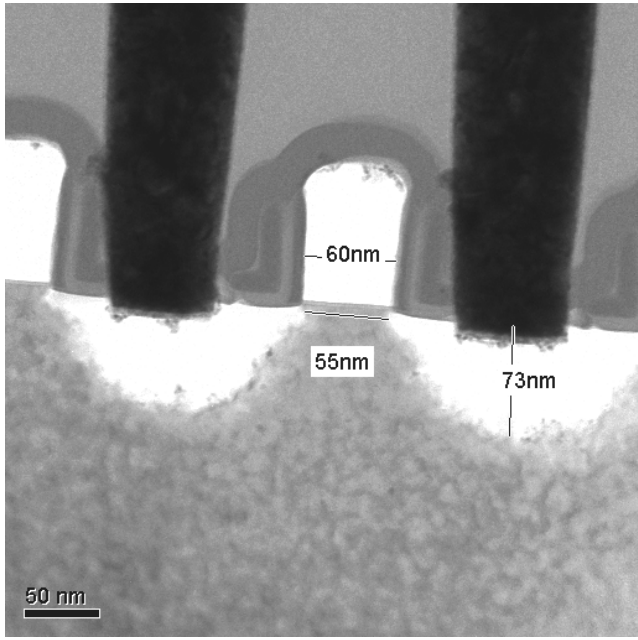
- Junction stained Transmission Electron Micrographs of transistor gates



130 nm technology



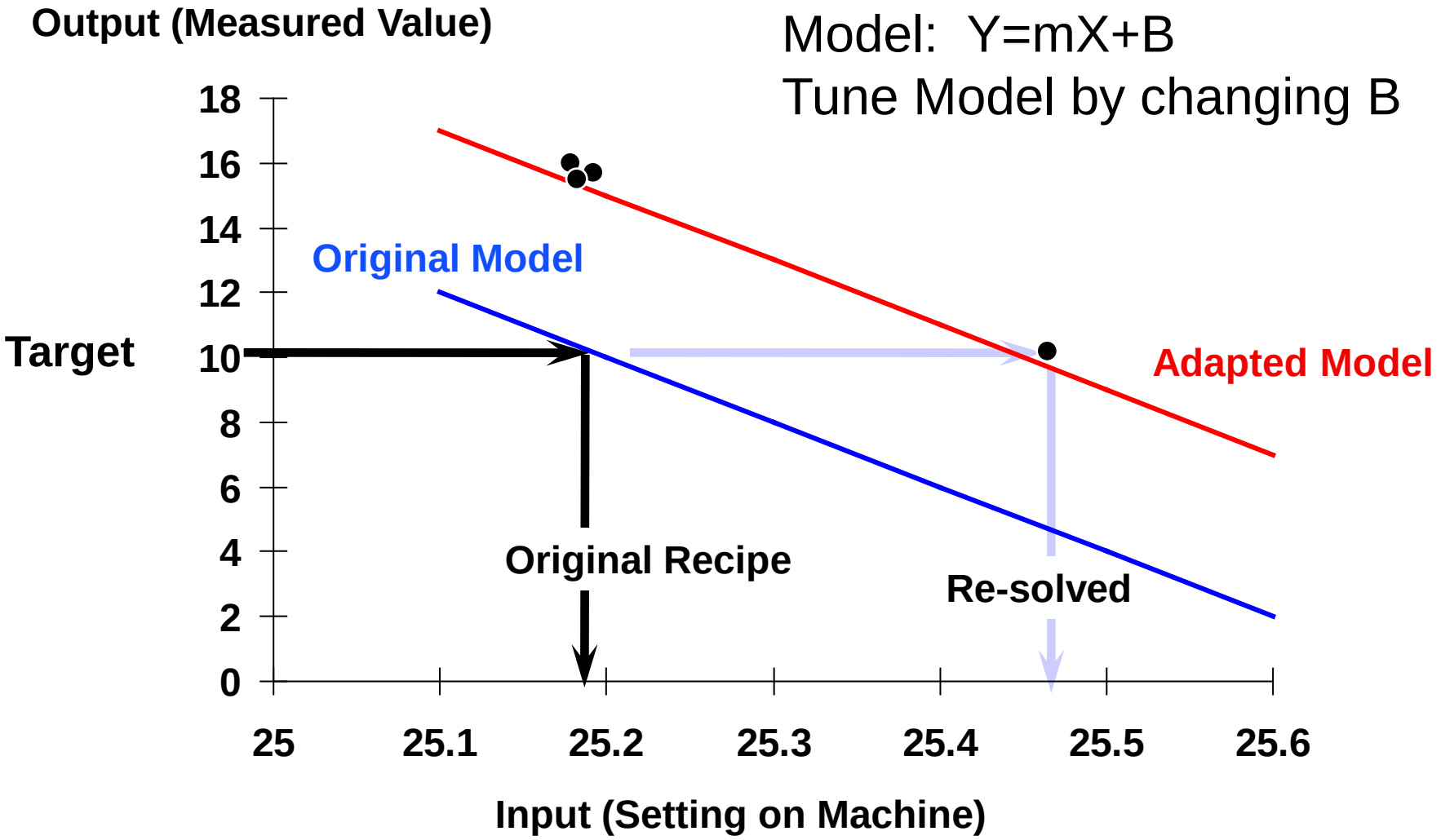
90 nm technology



65 nm technology

Fib prepared TEM cross section NMOS

Generic APC Model

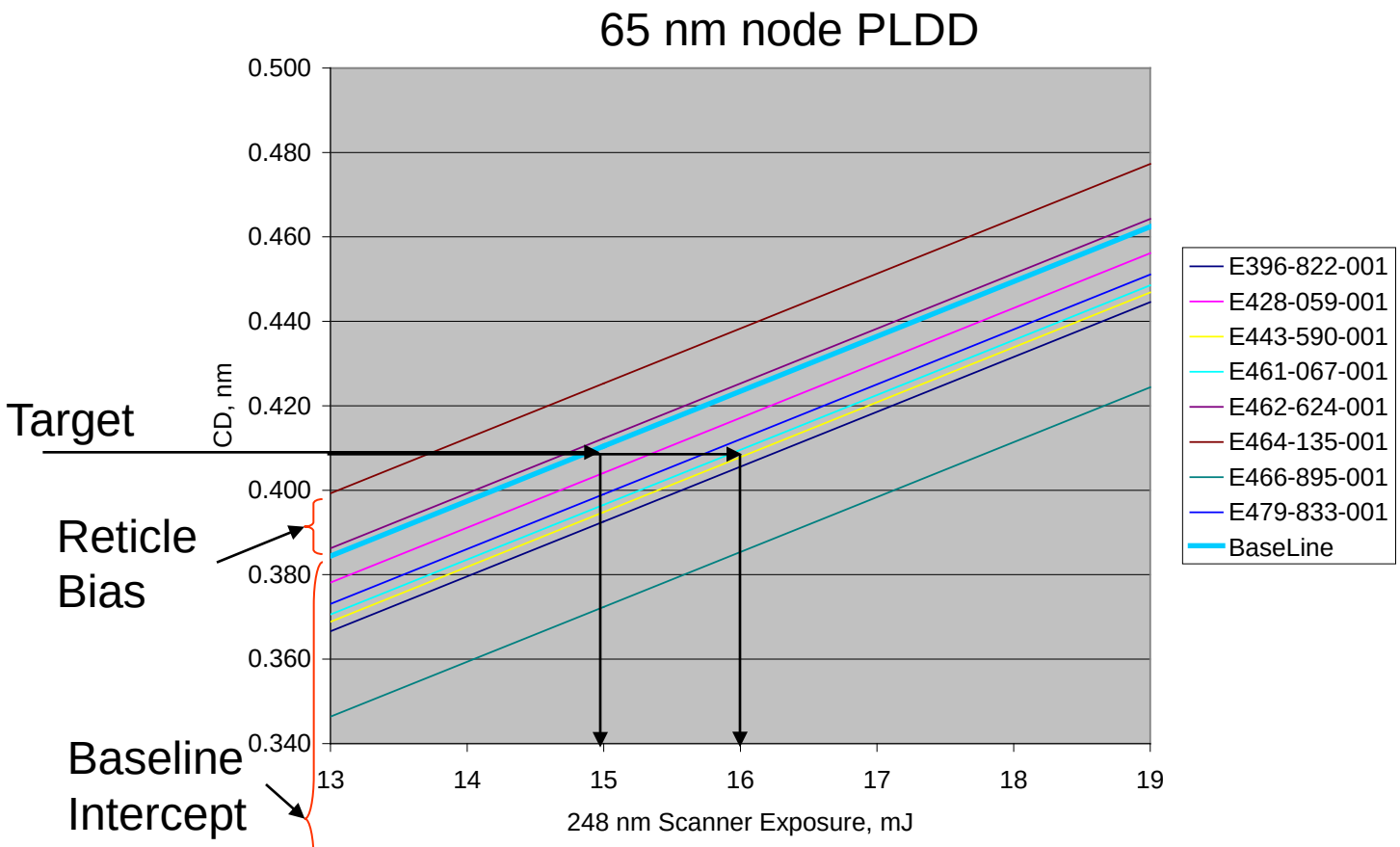


EWMA Tuner

- Define error term
  - $e = Y - (mX + B)$
- $B(i+1) = B(i) + (1-\lambda)*e$
- Track only the most recent value for B
- Works in open loop and closed loop
- Fairly insensitive to out of sequence and missing measurements
- Filter factor λ can be dynamic, based on context and/or output variance

Photo Exposure Example

- A baseline is maintained for each resist at each logpoint
- “High Mix” with several products offset from the baseline
- Baseline is tuned with EWMA
- Reticle offsets have dynamic gain tuning



Lessons Learned

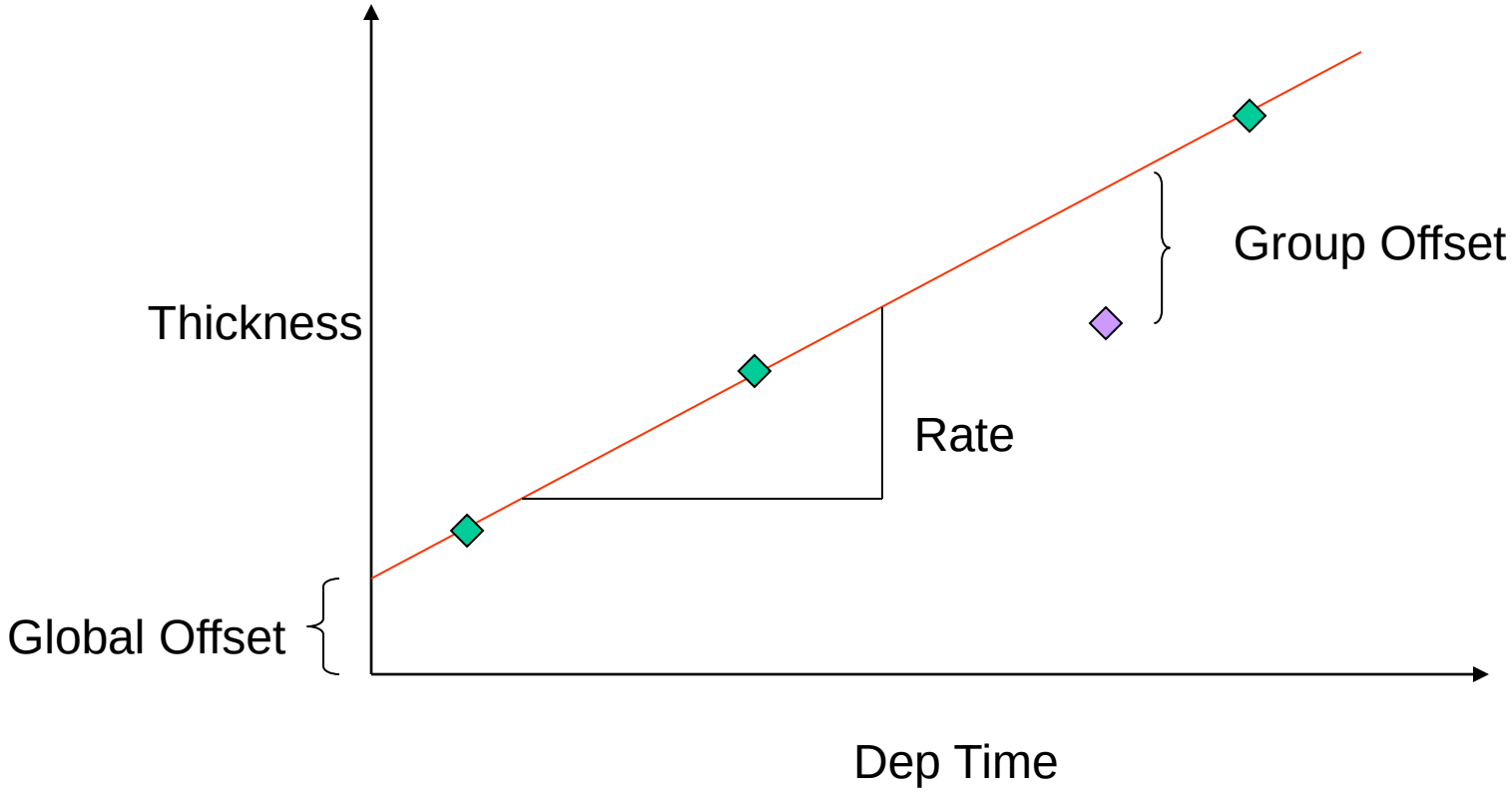
- What constitutes a new baseline?
  - Layer, resist, substrate, illumination mode
- How should the error be partitioned between the machine and product offsets?
- Offsets from reticle to reticle should be fixed, however
  - Learning an offset during a machine step/drift results in an incorrect bias estimation for low volume devices
  - Estimated Reticle biases must continue to float forever

Thin Film Deposition

- Maintain a model that will deliver a continuum of thicknesses
- Often times in practice, metrology precision is prioritized
- This can necessitate metrology offsets for some films
- Accuracy needs to be emphasized for thin film metrology

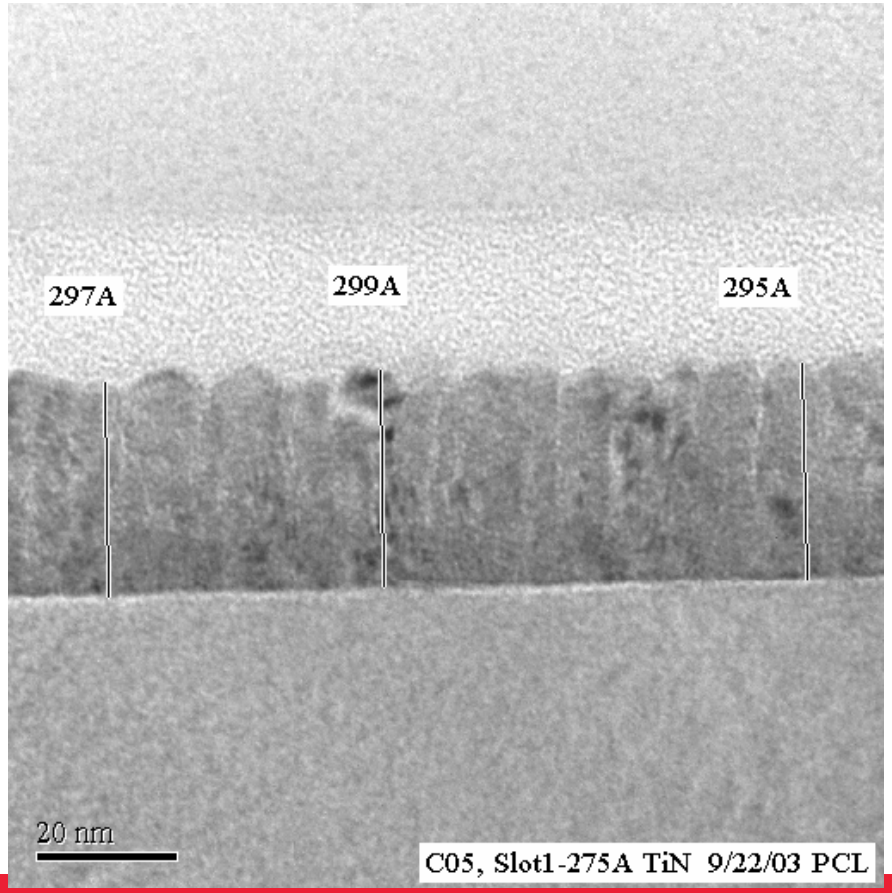
Metrology Offset Graph

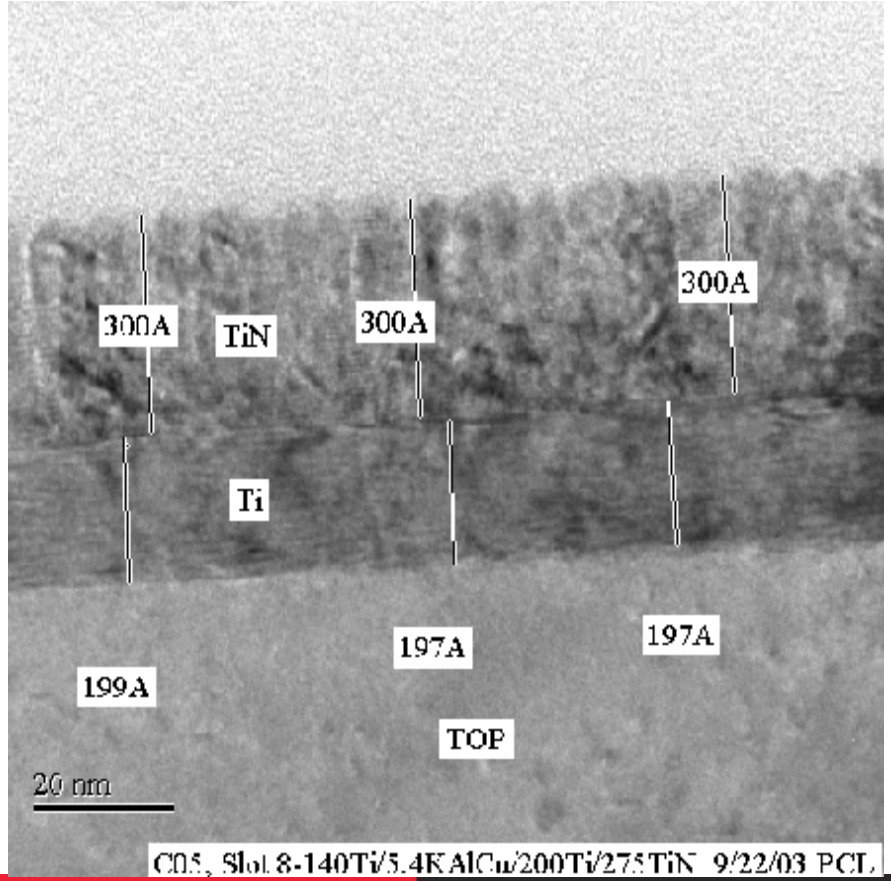
- Apply offset to bring measurement into common model



Metrology Offset Picture

- Same TiN film in two stacks, different thickness value from metrology tool





Control Loop Scaling

- Photo Alignment for Scanners
  - 10 inputs and outputs
  - 20 scanners
  - 40 layers
  - 100 products
  - Up to 800,000 SISO loops in one control strategy document
  - In practice, this is a sparse matrix

Economic Impact of APC

- Increase yield
  - Higher selling price for better transistor performance
  - Improved Interconnect RC Control
- Reduce scrap
  - Lower scrap for leakage current
  - Reduce inline excursions
- Increase Equipment availability
  - Reduce rework, test wafers, pilot wafers
  - Increase time between SPC failures, change notices
- Reduce cycle time
  - Reduce rework, test wafers

The Beginning of APC in Semi's

- TI's study of microelectronics manufacturing science and technology (MMST program) began in 1988, ended in 1994/5
- Stephanie (Watts) Butler was involved in supervisory (Run-to-run) control
- Terence Breedijk was involved with real-time tool control
- ProcessWORKS software was invented during this program, later commercialized through Adventa, now owned by Rudolph Technologies

Explosive Growth in APC

- Steph Butler put together a group of APC engineers inside TI ~1996
  - Scott Bushman
  - John Stuber
  - Other people not supervised by TFE
- APC becomes required for gate CD control in the 0.35 um node
- Required for photolithography in 0.25 um node
- Over 150 control points in the 65 nm node
- Retrofitted into all TI fabs over several years
- Will be required in fabs purchased by TI

University Research Essential

- Central APC group was disbursed when TI sells memory business to Micron in 1998
  - Each TI fab picks up individuals to support APC
  - Software developers spun off as Adventa
- TI joins the Texas Modeling and Control Consortium (TMCC) in 2000
- Support for APC research doubled under the AMC umbrella in 2006
- A third student is supported by NSF under GOALI starting 2009

TFE's Diverse Research Topics

- Dealing with unobservability when estimating tool and product states
- Electrical Parameter Control
- Dynamic Sampling

- Virtual metrology
- Controller performance monitoring
- Building energy optimization

Control Performance Assessment (CPA) of Semiconductor Processes

- **Achievements:**

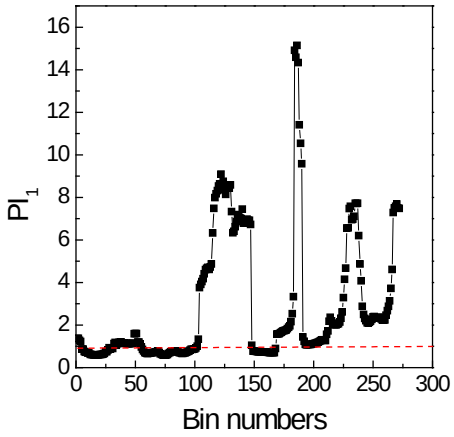
Xiaojing Jiang (UT-Austin)

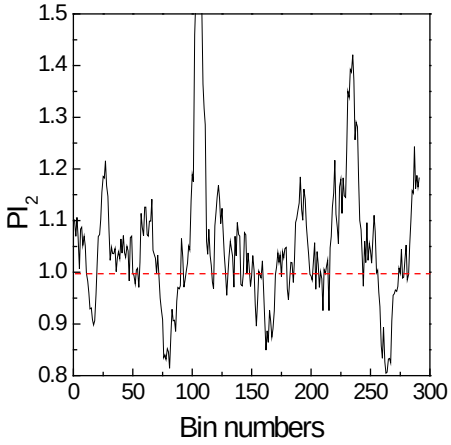
1) Developed and evaluated performance indices (PI_1 and PI_2) based on the closed-loop identification of the run-to-run control loops;
2) Incorporated autocorrelation analysis to determine effects of operating parameters;

- **Future plans:**

Apply CPA to high-mix processes

1) Threaded: Check every thread to assess performance
2) Non-threaded: Apply CPA for different targets and products





$$PI_1 = \frac{1}{\sqrt{\mathrm{var}(\hat{m}/m)}}$$

New

$$PI_2 = \frac{\mathrm{var}(y)}{\mathrm{var}(\varepsilon)}$$

Traditional

Building Energy Optimization

- CleanCalc II used for simulator
- Objective function = total annual electric energy
- Constraints in deg F
  - Air handler exit air temp – cooling mode $65 \leq x \leq 71$
  - Air handler exit air temp – heating mode $56 \leq y \leq 61$
  - Air handler exit air dew point $45 \leq z \leq 50$
- Initially (x,y,z) = (68, 59, 50)
  - Energy (i) = 159,865,060 kWh
- Nelder-Mead algorithm Converges at (66.1493, 59.6906, 49.7385)
  - Energy (m) = 159,251,473 kWh
  - Takes 16 iterations

Kriti Kapoor

Summary

- Inside TI, APC is a function of Process Engineering
- Processes without feedback are not “uncontrolled”
- A generic APC algorithm works for many fab processes
  - The challenge is to define the context information correctly
- APC has clear and significant economic impact to a fab
- APC Technology Advances will be made through University research